	L #	Hits	Search Text	DBs
1	L1	29365	(dependen$3 conflict$3) near10 (bit flag tag field)	USPAT; US-PGPUB
2	L3	4535	(dependen$3 conflict$3) near10 (bit flag tag field)	EPO; JPO; DERWENT; IBM_TDB
3	L8	173	1 near99 (flush$3 pipelin$3)	USPAT; US-PGPUB
4	L9	78	(renam$3 reorder$3) and 8	USPAT; US-PGPUB
5	L10	14	3 near99 (flush$3 pipelin$3)	EPO; JPO; DERWENT; IBM_TDB
6	L15	148	(renam$3 reorder$3) near99 1	USPAT; US-PGPUB
7	L16	58	15 and (flush$3 near10 pipelin$3)	USPAT; US-PGPUB
8	L17	10	(renam$3 reorder$3) near99 3	EPO; JPO; DERWENT; IBM_TDB

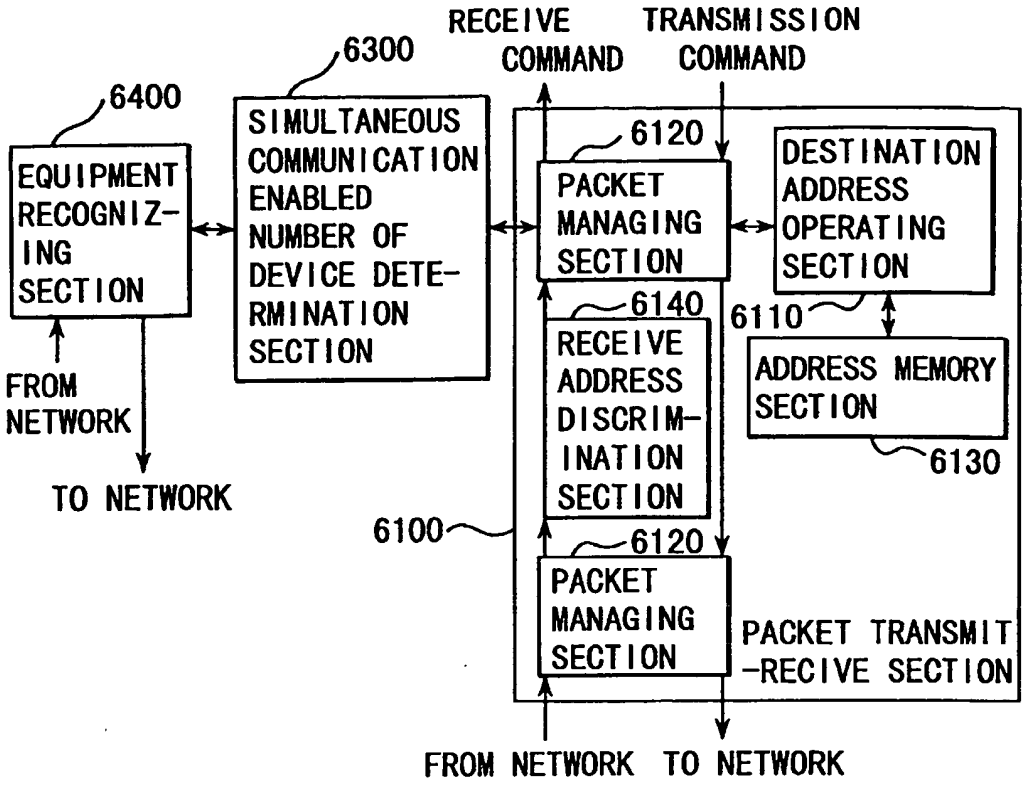
RECEIVE COMMAND
TRANSMISSION COMMAND
6300
6400
SIMULTANEOUS COMMUNICATION ENABLED NUMBER OF DEVICE DETE-RMINATION SECTION
EQUIPMENT RECOGNIZ-ING SECTION
FROM NETWORK
TO NETWORK
6120
PACKET MANAGING SECTION
DESTINATION ADDRESS OPERATING SECTION
6110
6140
RECEIVE ADDRESS DISCRIM-INATION SECTION
ADDRESS MEMORY SECTION
6130
6100
6120
PACKET MANAGING SECTION
PACKET TRANSMIT -RECIVE SECTION
FROM NETWORK
TO NETWORK

FIG. 63

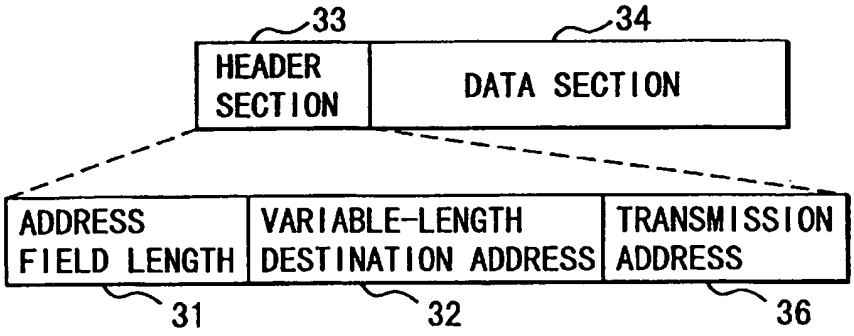
33
34
HEADER SECTION
DATA SECTION
ADDRESS FIELD LENGTH
VARIABLE-LENGTH DESTINATION ADDRESS
TRANSMISSION ADDRESS
31
32
36

FIG. 64

	Document ID	U	Title	Current OR
1	US 20040 03990 3 A1	☐	Multistandard video decoder and decompression system for processing encoded bit streams including a video formatter and methods relating thereto	712/300
2	US 20040 02500 0 A1	☒	Multistandard video decoder and decompression system for processing encoded bit streams including start code detection and methods relating thereto	712/300
3	US 20040 01977 5 A1	☒	Multistandard video decoder and decompression system for processing encoded bit streams including tokens and methods relating thereto	712/300
4	US 20030 22796 9 A1	☒	Multistandard video decoder and decompression system for processing encoded bit streams including a reconfigurable processing stage and methods relating thereto	375/240 .1
5	US 20030 19607 8 A1	☒	Data pipeline system and data encoding method	712/300
6	US 20030 18254 4 A1	☒	Multistandard video decoder and decompression system for processing encoded bit streams including a decoder with token generator and methods relating thereto	712/300
7	US 20030 15665 2 A1	☒	Multistandard video decoder and decompression system for processing encoded bit streams including a video formatter and methods relating thereto	375/240 .26
8	US 20030 14986 5 A1	☒	Processor that eliminates mis-steering instruction fetch resulting from incorrect resolution of mis-speculated branch instructions	712/244
9	US 20030 14986 2 A1	☒	Out-of-order processor that reduces mis-speculation using a replay scoreboard	712/217
10	US 20030 07911 7 A1	☒	Multistandard video decoder and decompression method for processing encoded bit streams according to respective different standards	712/300
11	US 20030 01888 4 A1	☒	Multistandard video decoder and decompression system for processing encoded bit streams including expanding run length codes and methods relating thereto	712/300
12	US 20020 15236 9 A1	☒	Multistandard video decoder and decompression system for processing encoded bit streams including storing data and methods relating thereto	712/300
13	US 20020 08781 0 A1	☒	System and method for high performance execution of locked memory instructions in a system with distributed memory and a restrictive memory model	711/145
14	US 20020 08330 4 A1	☒	Rename finish conflict detection and recovery	712/218
15	US 20020 06600 7 A1	☒	Multistandard video decoder and decompression system for processing encoded bit streams including pipeline processing and methods relating thereto	712/300
16	US 66979 30 B2	☒	Multistandard video decoder and decompression method for processing encoded bit streams according to respective different standards	712/2
17	US 66549 21 B1	☒	Decoding data from multiple sources	714/746
18	US 66041 90 B1	☒	Data address prediction structure and a method for operating the same	712/207

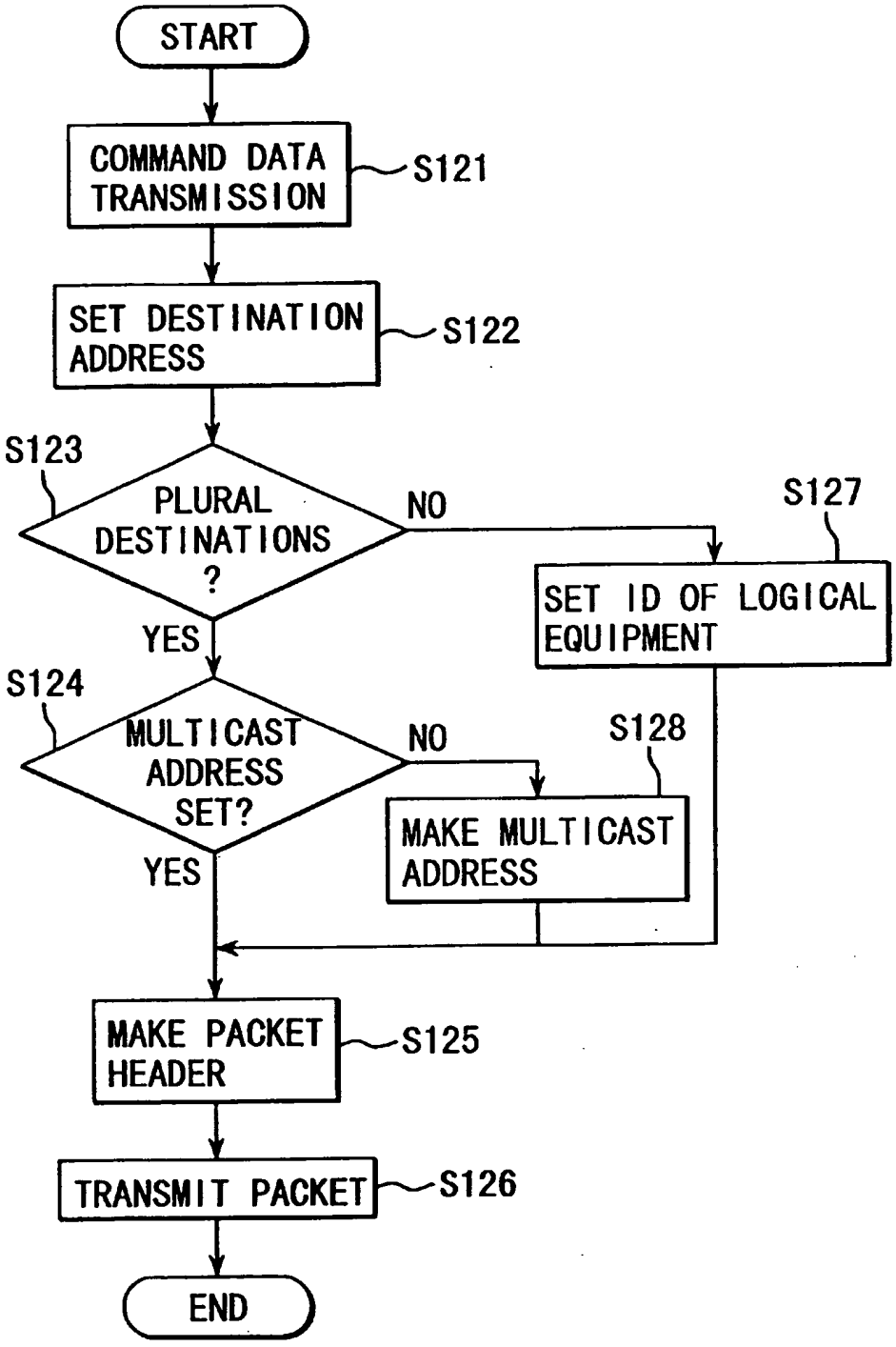
START
COMMAND DATA TRANSMISSION
S121
SET DESTINATION ADDRESS
S122
S123
PLURAL DESTINATIONS ?
NO
S127
SET ID OF LOGICAL EQUIPMENT
YES
S124
MULTICAST ADDRESS SET?
NO
S128
MAKE MULTICAST ADDRESS
YES
MAKE PACKET HEADER
S125
TRANSMIT PACKET
S126
END

FIG. 55

	Document ID	U	Title	Current OR
19	US 6535972 B1	☒	Shared dependency checking for status flags	712/217
20	US 6499123 B1	☒	Method and apparatus for debugging an integrated circuit	714/724
21	US 6463511 B2	☒	System and method for high performance execution of locked memory instructions in a system with distributed memory and a restrictive memory model	711/145
22	US 6446189 B1	☒	Computer system including a novel address translation mechanism	711/207
23	US 6435737 B1	☒	Data pipeline system and data encoding method	712/200
24	US 6393550 B1	☒	Method and apparatus for pipeline streamlining where resources are immediate or certainly retired	712/214
25	US 6393549 B1	☒	Instruction alignment unit for routing variable byte-length instructions	712/204
26	US 6330666 B1	☒	Multistandard video decoder and decompression system for processing encoded bit streams including start codes and methods relating thereto	712/300
27	US 6330665 B1	☒	Video parser	712/300
28	US 6275920 B1	☒	Mesh connected computed	712/14
29	US 6263422 B1	☒	Pipeline processing machine with interactive stages operable in response to tokens and system and methods relating thereto	712/209
30	US 6260189 B1	☒	Compiler-controlled dynamic instruction dispatch in pipelined processors	717/151
31	US 6219773 B1	☒	System and method of retiring misaligned write operands from a write buffer	711/201
32	US 6212629 B1	☒	Method and apparatus for executing string instructions	712/241
33	US 6212628 B1	☒	Mesh connected computer	712/226
34	US 6173388 B1	☒	Directly accessing local memories of array processors for improved real-time corner turning processing	712/22
35	US 6112017 A	☒	Pipeline processing machine having a plurality of reconfigurable processing stages interconnected by a two-wire interface bus	712/200
36	US 6079009 A	☒	Coding standard token in a system compromising a plurality of pipeline stages	712/209
37	US 6067417 A	☒	Picture start token	712/18
38	US 6047112 A	☒	Technique for initiating processing of a data stream of encoded video information	714/1
39	US 6038380 A	☒	Data pipeline system and data encoding method	712/200
40	US 6035126 A	☒	Data pipeline system and data encoding method	712/29

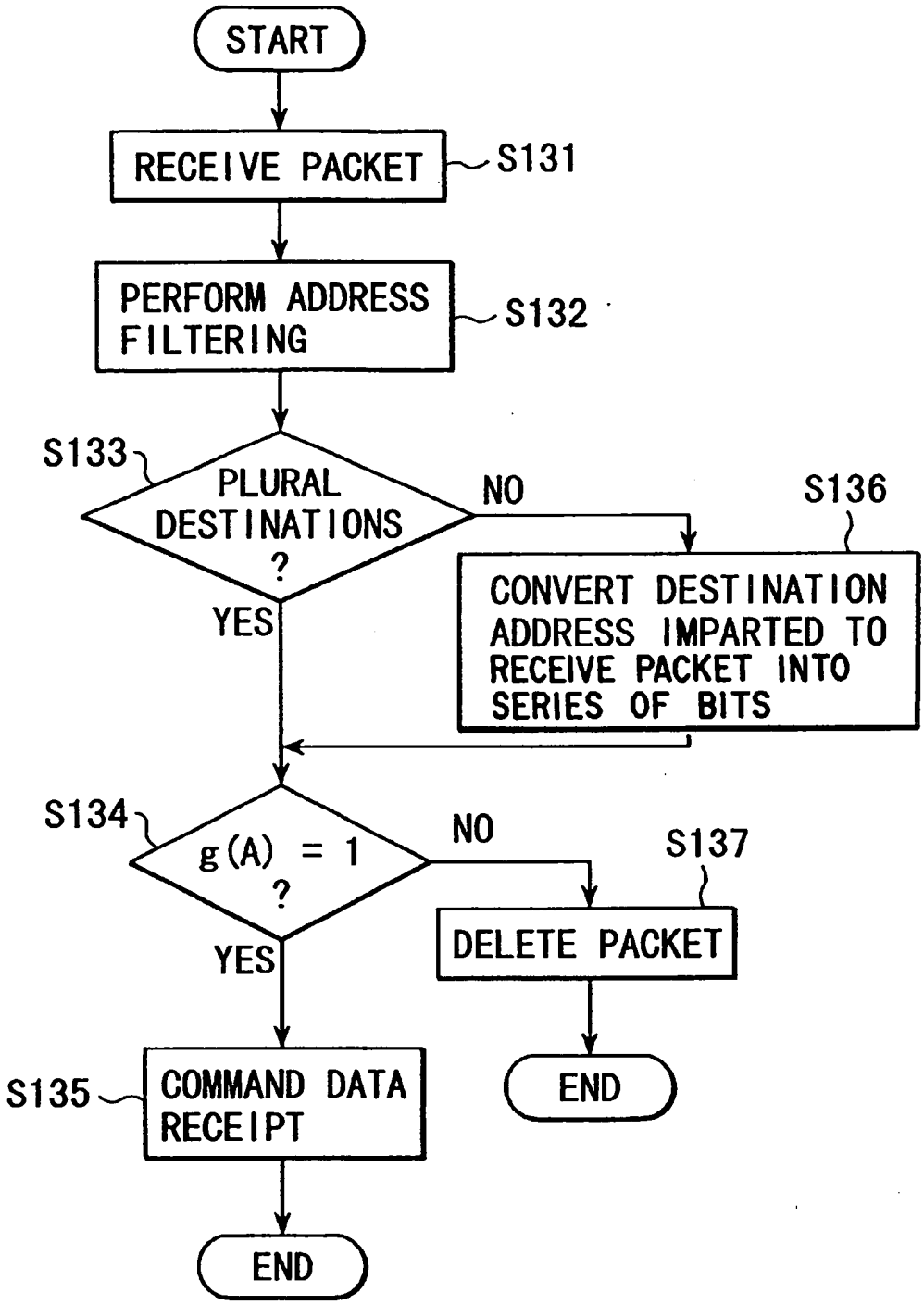
START
RECEIVE PACKET
S131
PERFORM ADDRESS FILTERING
S132
S133
PLURAL DESTINATIONS ?
NO
S136
YES
CONVERT DESTINATION ADDRESS IMPARTED TO RECEIVE PACKET INTO SERIES OF BITS
S134
g(A) = 1 ?
NO
S137
YES
DELETE PACKET
S135
COMMAND DATA RECEIPT
END
END

FIG. 56

	Document ID	U	Title	Current OR
41	US 6018776 A	☒	System for microprogrammable state machine in video parser clearing and resetting processing stages responsive to flush token generating by token generator responsive to received data	710/7
42	US 6006324 A	☒	High performance superscalar alignment unit	712/204
43	US 5987595 A	☒	Method and apparatus for predicting when load instructions can be executed out-of order	712/216
44	US 5978592 A	☒	Video decompression and decoding system utilizing control and data tokens	712/1
45	US 5968169 A	☒	Superscalar microprocessor stack structure for judging validity of predicted subroutine return addresses	712/239
46	US 5956519 A	☒	Picture end token in a system comprising a plurality of pipeline stages	712/16
47	US 5907860 A	☒	System and method of retiring store data from a write buffer	711/117
48	US 5887152 A	☒	Load/store unit with multiple oldest outstanding instruction pointers for completing store and load/store miss instructions	712/217
49	US 5881301 A	☒	Inverse modeller	712/1
50	US 5848433 A	☒	Way prediction unit and a method for operating the same	711/137
51	US 5842033 A	☒	Padding apparatus for passing an arbitrary number of bits through a buffer in a pipeline system	712/1
52	US 5835740 A	☒	Data pipeline system and data encoding method	712/200
53	US 5832297 A	☒	Superscalar microprocessor load/store unit employing a unified buffer and separate pointers for load and store operations	710/5
54	US 5832249 A	☒	High performance superscalar alignment unit	712/204
55	US 5822574 A	☒	Functional unit with a pointer for mispredicted resolution, and a superscalar microprocessor employing the same	712/233
56	US 5822558 A	☒	Method and apparatus for predecoding variable byte-length instructions within a superscalar microprocessor	712/213
57	US 5819059 A	☒	Predecode unit adapted for variable byte-length instruction set processors and method of operating the same	712/213
58	US 5819057 A	☒	Superscalar microprocessor including an instruction alignment unit with limited dispatch to decode units	712/204
59	US 5813033 A	☒	Superscalar microprocessor including a cache configured to detect dependencies between accesses to the cache and another cache	711/144
60	US 5809070 A	☒	Inverse quantizer	712/200
61	US 5805914 A	☒	Data pipeline system and data encoding method	382/232
62	US 5787474 A	☒	Dependency checking structure for a pair of caches which are accessed from different pipeline stages of an instruction processing pipeline	711/138

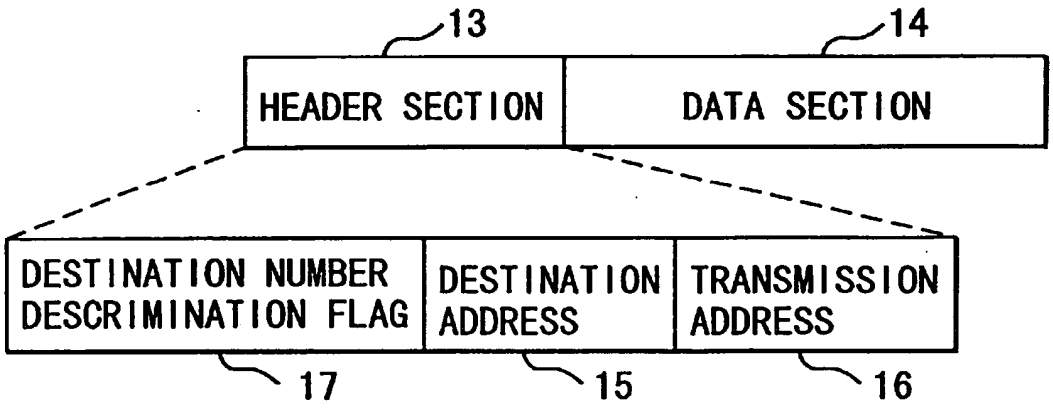
13
14
HEADER SECTION
DATA SECTION
DESTINATION NUMBER DESCRIMINATION FLAG
DESTINATION ADDRESS
TRANSMISSION ADDRESS
17
15
16

FIG. 57

	Document ID	U	Title	Current OR
63	US 5784631 A	☒	Huffman decoder	382/246
64	US 5781753 A	☒	Semi-autonomous RISC pipelines for overlapped execution of RISC-like instructions within the multiple superscalar execution units of a processor having distributed pipeline control for speculative and out-of-order execution of complex instructions	712/218
65	US 5768610 A	☒	Lookahead register value generator and a superscalar microprocessor employing same	712/23
66	US 5768575 A	☒	Semi-Autonomous RISC pipelines for overlapped execution of RISC-like instructions within the multiple superscalar execution units of a processor having distributed pipeline control for sepculative and out-of-order execution of complex instructions	712/228
67	US 5768561 A	☒	Tokens-based adaptive video processing arrangement	710/63
68	US 5764946 A	☒	Superscalar microprocessor employing a way prediction unit to predict the way of an instruction fetch address and to concurrently provide a branch prediction address corresponding to the fetch address	712/239
69	US 5740398 A	☒	Program order sequencing of data in a microprocessor with write buffer	711/117
70	US 5737629 A	☒	Dependency checking and forwarding of variable width operands	712/23
71	US 5615402 A	☒	Unified write buffer having information identifying whether the address belongs to a first write operand or a second write operand having an extra wide latch	712/38
72	US 5603012 A	☒	Start code detector	712/208
73	US 5590352 A	☒	Dependency checking and forwarding of variable width operands	712/23
74	US 5588113 A	☒	Register file backup queue	714/15
75	US 5584009 A	☒	System and method of retiring store data from a write buffer	711/117
76	US 5553256 A	☒	Apparatus for pipeline streamlining where resources are immediate or certainly retired	712/217
77	US 5471598 A	☒	Data dependency detection and handling in a microprocessor with write buffer	711/122
78	US 4965724 A	☒	Compiler system using reordering of microoperations to eliminate interlocked instructions for pipelined processing of assembler source program	717/160

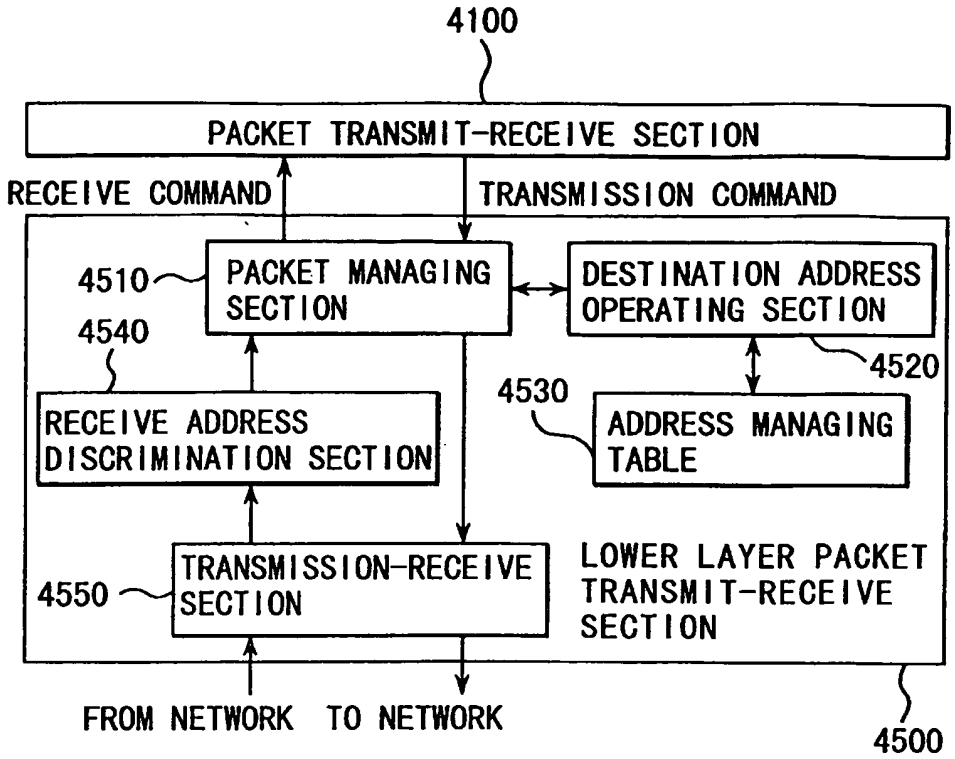

FIG. 58

LOGICAL EQUIPMENT ADDRESS	LOWER LAYER ADDRESS
1	532012
2	133434
3	200956
4	398067
⋮	⋮

FIG. 61

	Document ID	U	Title	Current OR
1	JP 63307 535 A	☐	PIPELINE CONTROL CIRCUIT	
2	JP 62175 831 A	☒	CONTROL SYSTEM FOR PIPELINE WITH TAG	
3	JP 58222 361 A	☒	CONTROL SYSTEM OF PRIORITY DECISION FOR ACCESS REQUEST IN DATA PROCESSING SYSTEM	
4	EP 61201 2 A1	☒	A pipeline computer with scoreboard.	
5	WO 93142 96 A1	☒	EQUIPMENT FOR CLEARING ROCK AND OTHER SURFACES OF STONE AND OTHER MATERIAL BY MEANS OF WATER JETS UNDER HIGH PRESSURE	
6	EP 40548 9 A2	☒	Resource conflict detection method and apparatus included in a pipelined processing unit.	
7	US 20020 12159 7 A	☒	Mass spectrometer system operation involves applying axial field and periodic flush pulse to processing section operated under suitable conditions	
8	US 20020 08330 4 A	☒	Out-of-order processor operation method involves providing separate logic for detecting dependency conflict associated with instruction which is to be currently executed to set conflict flag	
9	US 62634 24 B	☒	Multi-pipeline processor uses single port arithmetic logic unit in one pipeline to obtain carry bits of two port arithmetic unit in other pipeline which is processing arithmetically dependent pair of instructions	
10	US 62601 89 B	☒	Instruction processing method for digital data processor, involves compiling identified pipeline dependencies in multiple instructions and field of code block to control hardware-based dependency checking	
11	US 55599 87 A	☒	Updating Duplicate Tag cache status information in snooping bus protocol computer system - sends processor commands and addresses for modification of processor's Duplicate Tag status to address interface to system bus and updates status if no valid system bus commands and addresses are in interface pipeline	
12	US 54715 98 A	☒	Microprocessor with data dependency detection facility - has control logic comparing address fields in write buffer with read instructions to bypass write buffer data field to execution stage in pipelined core unit	
13	EP 40548 9 A	☒	Resource conflict appts. included in pipelined processing unit - for detecting and resolving conflicts in use of register and indicator resources during different phases of instruction execution	
14	WO 87006 58 A	☒	Priority resolution system for video display appts. - has priority logic units each effecting pipelines bit-wise comparison between input numbers	

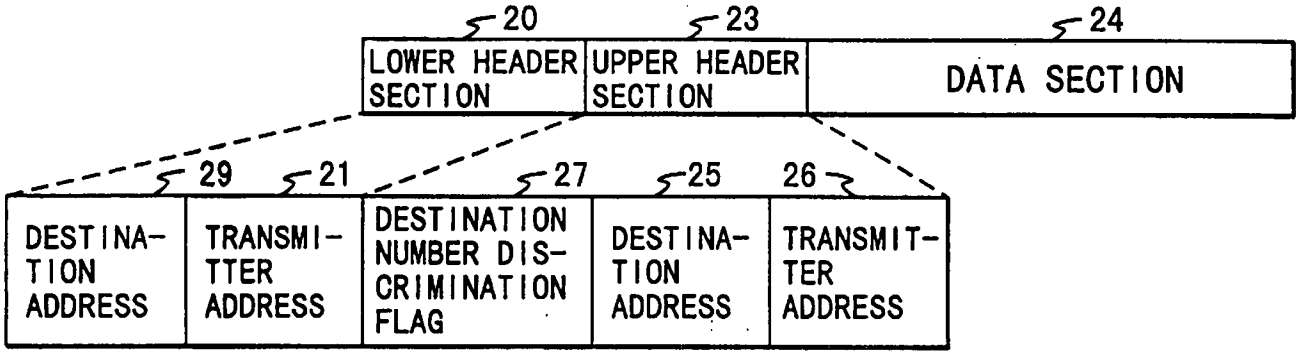
20
23
24
LOWER HEADER SECTION
UPPER HEADER SECTION
DATA SECTION
29
21
27
25
26
DESTINA-TION ADDRESS
TRANSMI-TTER ADDRESS
DESTINATION NUMBER DIS-CRIMINATION FLAG
DESTINA-TION ADDRESS
TRANSMIT-TER ADDRESS

FIG. 59

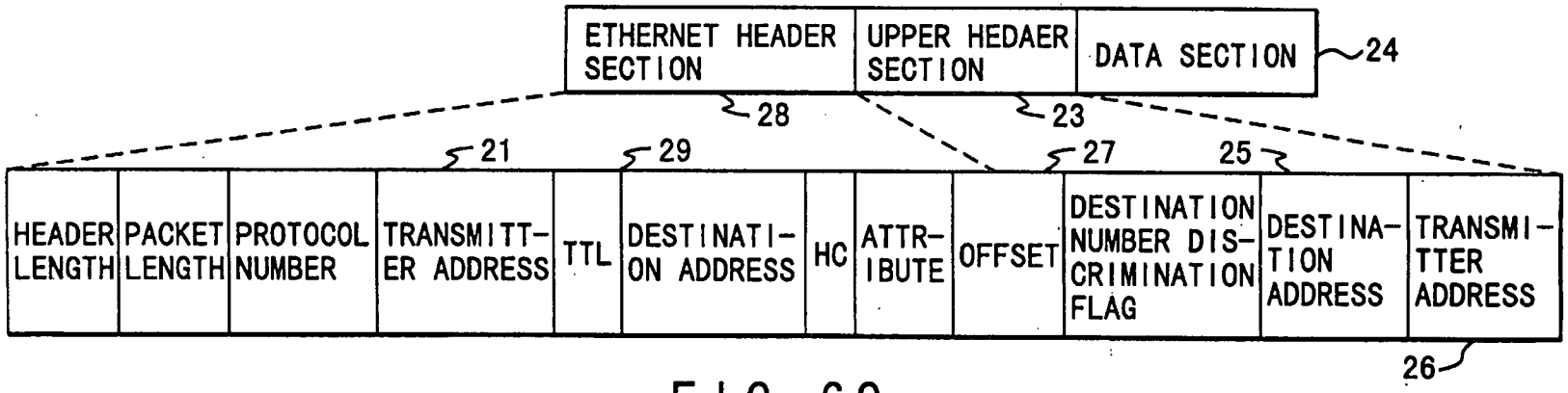
ETHERNET HEADER SECTION
UPPER HEDAER SECTION
DATA SECTION
24
28
23
21
29
27
25
HEADER LENGTH
PACKET LENGTH
PROTOCOL NUMBER
TRANSMITT-ER ADDRESS
TTL
DESTINATI-ON ADDRESS
HC
ATTR-IBUTE
OFFSET
DESTINATION NUMBER DIS-CRIMINATION FLAG
DESTINA-TION ADDRESS
TRANSMI-TTER ADDRESS
26

FIG. 60

	Document ID	U	Title	Current OR
1	JP 2000148486 A	☐	COMPUTER SYSTEM	
2	WO 9908185 A1	☒	A DEPENDENCY TABLE FOR REDUCING DEPENDENCY CHECKING HARDWARE	
3	EP 679991 A1	☒	Data processor for variable width operands.	
4	US 6490635 B	☒	Queued command conflict detection method for disk drive controller, involves setting conflict flag based on overlap between two different address ranges to restrict command reordering	
5	US 6209084 B	☒	Superscalar microprocessor has reorder buffer which assigns tags to respective source operand specifier in accordance with dependency information stored in dependency table	
6	WO 9908185 A	☒	Dependency checking apparatus for superscalar microprocessor	
7	EP 709769 A	☒	Pipeline microprocessor capable of issuing and executing multiple instructions - performs source operand dependency analysis, register re=naming and provides rapid pipeline recovery for microprocessor issuing and executing multiple instructions out of order in single machine cycle	
8	US 5371684 A	☒	Floor plan layout for register re-naming circuit - arranges data dependency comparator blocks in row and columns, and positions tag assignment logic in layout regions in blocks	
9	EP 636256 B	☒	Register re-naming system for use in super-scalar RISC computers - includes data check circuit determining data dependency, and tag assignment circuit generating operand location tags	
10	US 4965724 A	☒	Source program compiling method - using recording of microoperations to eliminate interlocked instructions for pipelined processing	

METHOD OF CONTROLLING A COMMUNICATION AND APPARATUS FOR THE SAME

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a communication control apparatus such that groups are formed by a plurality of portable information equipment and mutual communication is performed, and a method therefor.

2. Description of the Related Art

Hitherto, data transference between computers each having a communication function has mainly been performed by one-to-one communication. A most apparent typical example is data transference realized through a telephone line. To perform the communication through the telephone line, a user is needed to move to a place at which a telephone set is installed, and then instructs the telephone number intended to be communicated with. Therefore, only one-to-one communication with a person, the telephone number of which has been known, can be performed. Although use of a portable telephone results in a user being enabled to relatively freely hold communication in terms of the place for data transmission, the user is still needed to be capable of holding communication with a base station and to previously know the telephone number intended to be communicated while being limited to only the one-to-one communication.

Although broadcasting can be considered to realize one-to-multiple communication, broadcasting is able to basically realize only one directional communication.

Internet has been known to serve as a network exclusively used to realize communication among computers. Communication is realized in Internet by a technology called TCP/IP which uses IP address for specifying the terminal intended to be communicated, the IP address being address expressed by 32 bits and provided for each communication terminal. However, the communication using TCP/IP can be realized only when the communication terminals are connected by wire to one another. Thus, the foregoing communication cannot freely be used because of limitation of the places for use. Moreover, the IP address of the terminal intended to be communicated is needed to be known. In recent years, wireless LAN capable of realizing wireless computer communication has enabled the communication to be performed at arbitrary places. However, the necessity of previously knowing the IP address of the computer intended to be communicated cannot be eliminated.

As a technique capable of holding communication without the necessity of previously knowing the address of the terminal intended to be communication with, IrDA is available. IrDA is a communication technique using infrared rays and enabling data transmission to be performed simply by causing infrared-ray emitting and receiving portions of the own communication terminal to face the infrared-ray emitting and receiving portions of the communication terminal intended to be communicated. However, IrDA conveniently capable of eliminating the necessity of knowing the address of the other terminal is able to realize one-to-one communication. Thus, same information cannot be transmitted simultaneously to a plurality of persons.

As a means capable of solving the foregoing problem, a technique has been disclosed in Japanese Patent Laid-Open No. 7-336370 laid open on Dec. 22, 1995. According to the disclosure in Japanese Patent Laid-Open No. 7-336370, each

communication terminal spontaneously transmits information for identifying the own communication terminal. Each communication terminal recognizes communication-enabled terminals existing adjacent to the own terminal in accordance with ID information transmitted from other communication terminals. Then, instructed communication terminals form a group in which communication terminals therein can be multicast-supplied with same information.

By employing the technique disclosed in Japanese Patent Laid-Open No. 7-336370 in a portable information device having a wireless communication function, fixed facilities are not required and multiplicity-to-multiplicity (N-to-N) communication can be performed at any place without the necessity of previously knowing the address of other communication terminals.

The technique disclosed in Japanese Patent Laid-Open No. 7-336370 eliminates the necessity of providing fixed facilities as have been required for the conventional technique and the necessity of previously knowing the address of the terminal intended to be communicated with. The technique is able to realize communication whenever a user intends regardless of the place at which the communication is held. The foregoing technique is considered to be advantageous when combined with portable information devices having the wireless communication function.

The structure disclosed in Japanese Patent Laid-Open No. 7-33637 has not particularly limited a method of setting the address of the own terminal, that is, the identifier of the own terminal. Although a conventional method may be employed in which a server for setting the identifier is provided, there arises a problem in that communication can be performed only when the server exists. As a setting method which does not use a server, a method in which a user manually sets the identifier or a method in which random numbers generated by each terminal are used may be employed. However, an excessively large identifier space is required to prevent overlap of the identifiers of adjacent terminals regardless of the time and the place. However, use of the large identifier space encounters a problem of complicated handling and deterioration in the communication efficiency.

If a plurality of communication terminal identifiers accidentally coincide with one another, the communication terminals cannot be distinguished from one another. Thus, there arises a problem in that existence of only one communication terminal is recognized though a plurality of communication terminals exist in actual.

Since the communication-enabled terminals are recognized by always transmitting ID information of the own communication terminal and receiving communication terminal ID information transmitted from other communication terminals, great electric power is required in addition to that required to transmit data. This causes a critical problem for a portable information device to arise because of limitation of electric power allowed to be provided. Since communication terminal ID information is continuously transmitted during transmission of data, data transmission band is limited.

Since communication-enabled terminal is recognized in accordance with communication terminal ID information spontaneously transmitted from each terminal, whether communication can be held with a specific terminal is required to be determined after a sufficiently long time has elapsed for the terminal to transmit the communication terminal ID information. That is, the recognition process is performed on the initiative of the terminal to be recognized as compared with the terminal which recognizes the termi-

	Document ID	U	Title	Current OR
1	US 20020 08330 4 A1	☐	Rename finish conflict detection and recovery	712/218
2	US 20020 00745 0 A1	☒	Line-oriented reorder buffer	712/23
3	US 20010 03743 4 A1	☒	Store to load forwarding using a dependency link file	711/146
4	US 66622 80 B1	☒	Store buffer which forwards data based on index and optional way match	711/156
5	US 66041 90 B1	☒	Data address prediction structure and a method for operating the same	712/207
6	US 65499 90 B2	☒	Store to load forwarding using a dependency link file	711/146
7	US 65464 53 B1	☒	Proprammable DRAM address mapping mechanism	711/5
8	US 65429 86 B1	☒	Resolving dependencies among concurrently dispatched instructions in a superscalar microprocessor	712/217
9	US 65359 72 B1	☒	Shared dependency checking for status flags	712/217
10	US 64938 19 B1	☒	Merging narrow register for resolution of data dependencies when updating a portion of a register in a microprocessor	712/210
11	US 64738 37 B1	☒	Snoop resynchronization mechanism to preserve read ordering	711/146
12	US 64738 32 B1	☒	Load/store unit having pre-cache and post-cache queues for low latency load memory operations	711/118
13	US 64271 93 B1	☒	Deadlock avoidance using exponential backoff	711/146
14	US 64153 60 B1	☒	Minimizing self-modifying code checks for uncacheable memory types	711/139
15	US 63935 36 B1	☒	Load/store unit employing last-in-buffer indication for rapid load-hit-store	711/159
16	US 63816 89 B2	☒	Line-oriented reorder buffer configured to selectively store a memory operation result in one of the plurality of reorder buffer storage locations corresponding to the executed instruction	712/215
17	US 63398 22 B1	☒	Using padded instructions in a block-oriented cache	712/213
18	US 62928 84 B1	☒	Reorder buffer employing last in line indication	712/216
19	US 62667 44 B1	☒	Store to load forwarding using a dependency link file	711/146
20	US 62498 62 B1	☒	Dependency table for reducing dependency checking hardware	712/218
21	US 62370 82 B1	☒	Reorder buffer configured to allocate storage for instruction results corresponding to predefined maximum number of concurrently receivable instructions independent of a number of instructions received	712/215

nal. Therefore, appropriate adaptation required by the terminal which recognizes the other terminal cannot be satisfied, thus resulting in a problem to arise in that a satisfactory efficiency cannot be realized.

On the other hand, a conventional network consisting of information communication devices A, B, C, . . . , X as shown in FIG. 1 which are enabled to mutually transmit and receive information is arranged to transmit and receive packets by the following method.

A case will now be considered in which X is a transmitter, a terminal, to which information is intended to be transmitted, is selected from all of the terminals and information is transmitted by means of a packet having the packet structure as shown in FIG. 2. The packet consists of a data section 4 and a header section 3. The header section 3 includes two addresses, one of which is destination address 5 and another of which is transmitter address 6. When a packet of this type is transmitted in a usual network, the packet is transmitted to the address provided for the header section 3. Then, the receiving device checks the header of the supplied packet and enabled to receive the packet if the address is the own address.

If information is intended to be transmitted to one device, for example, device A, equipment address of the device A is given as described above when the packet is transmitted.

Some conventional methods to be employed when information is intended to be transmitted to a plurality of devices will now be described.

A method may be employed in which equipment address is added as all of the destination addresses similarly to the case where information is intended to be transmitted to one device, that is, one-to-one communication is repeated. Since the foregoing method has not the simultaneous information transmission function, it encounters a problem in that the number of packets to be transmitted increases if the destined devices increases and repetition of the procedure required to realize transmission results in an excessively long time being taken to complete the transmission.

Another method may be employed in which negotiation is performed between the transmitter and the receiver to set multicast address. An assumption is performed that receiving devices are devices A, B and C. Device X requires the receiving devices to set the multicast address. The multicast address determined by the transmission device X is set by the receivers, and then the receiving devices respectively return ack. When the transmission device X has received, from all of the devices A, B and C, ack indicating completion of setting of the multicast address, simultaneous information transmission is enabled. For example, Class D of IP address corresponds to this. A 28-bit group number is provided as the multicast address. Since this method requires only one packet to perform transmission, it is an advantageous method when the same information is simultaneously transmitted to a fixed device group. However, above-mentioned method needs the transmission device to require setting by transmitting, to all destined devices, a packet for requiring the negotiation formed by adding each address or the broadcast address. Since the multicast address must be changed whenever the destined device is changed, negotiation is required to determine the multicast address with a new device intended to be communicated. Therefore, there arises a problem in that an excessively long loss time involves to actually transmit data.

As a transmission method requiring only one packet without negotiation, a method is available in which equipment addresses of all transmission devices are added to the header of one packet when the packet is transmitted. However, the foregoing method involves the packet header being elongated excessively if the number of devices intended to be communicated increases, causing the overheader to be enlarged. Thus, there arises a problem in that the execution throughput is reduced.

Another method capable of transmitting information with one packet without negotiation is a method using broadcast address. The above-mentioned method enables transmission to the overall device group, to which same information can be transmitted simultaneously, to be performed while requiring a fixed header length regardless of the number of the devices intended to be communicated. Therefore, the problem of the overhead can be solved. However, the foregoing method does not permit communication with a plurality of specific devices in the device group. Thus, the method encounters a problem in that the foregoing method is repeated unintentionally.

As described above, the conventional packet transmitting and receiving method requires the transmission device to perform negotiation with the destined device to transmit information after the multicast address has been set to the transmitting device and the receiving device. Moreover, the receiving device is required to set the multicast address. Thus, the procedure has been too complicated and a long time has been required. In the case where all addresses are arranged to form an address section, increase in the addresses causes the length of the packet header to be elongated excessively. Thus, there arises a problem in that the overhead is enlarged excessively.

SUMMARY OF THE INVENTION

A first object of the present invention is to provide a communication control apparatus and a method therefor enabling each terminal in a certain group of communication terminals to automatically set a terminal identifier with which each terminal can uniquely be identified.

A second object of the present invention is to detect coincidence of a communication terminal identifier of each of the own terminals and the identifiers of other communication terminals so as to prevent overlap of ID information.

A third object of the present invention is to perform reliable communication among a plurality of adjacent communication terminals with small electric power.

A fourth object of the present invention is to multicast a specific communication terminal among a plurality of adjacent communication terminals with small electric power.

A fifth object of the present invention is to, in accordance with a requirement, quickly and more accurately, recognize communication-enabled terminal.

A sixth object of the present invention is to realize more flexible and efficient multicast address communication.

To achieve the first object, a communication control apparatus according to the present invention comprises:

receive means for receiving terminal ID information having information of another terminal transmitted from one or a plurality of other terminals with which communication is being held; and

own terminal identifier setting means for setting, to be an own terminal identifier, one of a plurality of terminal identifiers except the terminal identifiers of other terminals obtained from all of terminal ID information items received from the receive means and previously set and enabled to be used to perform the communication.

	Document ID	U	Title	Current OR
22	US 6212621 B1	☒	Method and system using tagged instructions to allow out-of-program-order instruction decoding	712/212
23	US 6209084 B1	☒	Dependency table for reducing dependency checking hardware	712/233
24	US 6189089 B1	☒	Apparatus and method for retiring instructions in excess of the number of accessible write ports	712/218
25	US 6185675 B1	☒	Basic block oriented trace cache utilizing a basic block sequence buffer to indicate program order of cached basic blocks	712/238
26	US 6134651 A	☒	Reorder buffer employed in a microprocessor to store instruction results having a plurality of entries predetermined to correspond to a plurality of functional units	712/215
27	US 6108769 A	☒	Dependency table for reducing dependency checking hardware	712/216
28	US 6032251 A	☒	Computer system including a microprocessor having a reorder buffer employing last in buffer and last in line indications	712/216
29	US 6026482 A	☒	Recorder buffer and a method for allocating a fixed amount of storage for instruction results independent of a number of concurrently dispatched instructions	712/215
30	US 5983342 A	☒	Superscalar microprocessor employing a future file for storing results into multiportion registers	712/218
31	US 5968169 A	☒	Superscalar microprocessor stack structure for judging validity of predicted subroutine return addresses	712/239
32	US 5961634 A	☒	Reorder buffer having a future file for storing speculative instruction execution results	712/218
33	US 5922069 A	☒	Reorder buffer which forwards operands independent of storing destination specifiers therein	712/217
34	US 5920710 A	☒	Apparatus and method for modifying status bits in a reorder buffer with a large speculative state	712/216
35	US 5903741 A	☒	Method of allocating a fixed reorder buffer storage line for execution results regardless of a number of concurrently dispatched instructions	712/218
36	US 5903740 A	☒	Apparatus and method for retiring instructions in excess of the number of accessible write ports	712/217
37	US 5901302 A	☒	Superscalar microprocessor having symmetrical, fixed issue positions each configured to execute a particular subset of instructions	712/215
38	US 5887152 A	☒	Load/store unit with multiple oldest outstanding instruction pointers for completing store and load/store miss instructions	712/217
39	US 5884061 A	☒	Apparatus to perform source operand dependency analysis perform register renaming and provide rapid pipeline recovery for a microprocessor capable of issuing and executing multiple instructions out-of-order in a single processor cycle	712/217
40	US 5878244 A	☒	Reorder buffer configured to allocate storage capable of storing results corresponding to a maximum number of concurrently receivable instructions regardless of a number of instructions received	712/218
41	US 5872951 A	☒	Reorder buffer having a future file for storing speculative instruction execution results	712/218
42	US 5870580 A	☒	Decoupled forwarding reorder buffer configured to allocate storage in chunks for instructions having unresolved dependencies	712/218

To achieve the second object, the present invention has a structure such that own terminal ID information setting means sets own terminal ID information for determining the own communication terminal. Own terminal ID information is obtained from means for memorizing own terminal ID information to transmit it as existence information of the own terminal. Existence information receive means receives existence information from another communication terminal. In a case where received existence information and own terminal ID information coincide with each other, own terminal ID information changing means determines whether own terminal ID information is changed and changes it, if necessary.

To achieve the third object, the present invention has a structure such that ID imparting means imparts ID information of a packet to a transmission packet. Packet transmission means broadcasts packet to which ID has been imparted. Packet receive means receives broadcasted packet. Confirmation packet receipt number setting means sets the number of receipt confirmation packets to be received with respect to transmitted packets. Confirmation packet received number counting means counts the number of receipt confirmation packets with respect to transmitted packets. In a case where re-transmission means cannot receive receipt confirmation packets by a number to be received in a predetermined time, the same packet is transmitted again. In a case where receipt confirmation packet generating means has received a packet except the receipt confirmation packet, it generates a packet having ID information of the received packet and information indicating that the packet is a receipt confirmation packet.

To achieve the fourth object, the present invention has a structure such that address information receive means receives address information indicating existence of certain address and attribute of the address. Address selection means selects one or a plurality of addresses from received address information. Information receive means receives information transmitted to the selected address. Information transmission means transmits information to the selected address. Address generating means generates new address. Address transmission means transmits address information.

To achieve the fifth object, the present invention has a structure such that own terminal ID information setting means sets own terminal ID information for discriminating the own communication terminal. Own terminal ID information memory means memorizes the own terminal discrimination information. Existence confirmation information transmission means transmits existence confirmation information for recognizing communication-enabled terminals existing around the own terminal. Existence confirmation information receive means receives existence confirmation information transmitted from another communication terminal. Existence confirmation response transmission means transmits existence confirmation response for indicating existence of a coincidence terminal in a case where received existence confirmation information and own terminal ID information coincide with each other. Communication-enabled terminal recognizing means recognizes communication-enabled terminals existing around the own terminal in accordance with existence confirmation information and existence confirmation response transmitted from the own terminal or another terminal. Group setting means sets one or a plurality of communication terminals among recognized communication-enabled terminals into one group. Information transmission means transmits same type information to communication terminals belonging to a set group.

To achieve the sixth object, the present invention has a structure such that multiple address calculated from addresses of device groups with which transmission can be performed and address of the destined terminal is imparted to a packet header to be transmitted. The receive side is required to memorize only the address of the own device so that information destined to the own terminal is determined and information is received. Therefore, labor and time of negotiation can be saved efficiently. Since only one packet is required to be transmitted, enlargement of traffic can be prevented. In a case where information is transmitted to one terminal, the destination address in the form of the equipment address is as it is transmitted. Therefore, address calculation can be decreased and the time required to set transmission can further be shortened. A lower device for receiving a packet transmitted from the foregoing packet transmitting and receiving apparatus to transmit it while imparting the address sets broadcast address when information is transmitted to a plurality of devices and sets unicast address when information is transmitted to one device. Thus, the unicast communication to be performed when transmission is performed to a plurality of devices is repeated. The necessity of arranging the equipment addresses of the destined devices in the header can be eliminated. Moreover, since a lower device for receiving information is able to delete packets which are not destined to the own terminal and which are not required, the load for the upper device required to receive information can be reduced.

Since the header of the destined terminal has a variable length, communication with a multiplicity of devices with which multiple communication can be performed can be realized without a limitation of the number of the device. If the number of devices, with which communication is being held is small, only a short header is required.

A packet transmitting and receiving apparatus for achieving the sixth object comprises an address memory section for memorizing logical equipment address and the like of an own device and a destined device having an address field having a fixed length; a destination address operating section using logical address information of the address memory section to determine destination address having the address field having the fixed length of the destination packet, a packet generating section for generating a packet formed by imparting destination address generated by the destination address operating section to a header; and a receive address discrimination section for discriminating whether the supplied packet is destined to the own terminal, wherein the destination address is set to multicast address calculated from the equipment addresses of all or a portion of devices, which are the subject of communication, and the own equipment address so as to be transmitted, and the receive side uses all or a portion of the multicast address imparted to the receive packet, the destination address and the own equipment address of the own device to determine whether information is addressed to the own device so that only information addressed to the own device is acquired.

There is provided a transmission and receipt method having an arrangement such that, in a case where the number of destination is one, a destination device number discrimination flag is provided for the header of a destination packet to set the flag to indicate one destination so that the destination address is enabled to be transmitted in the form of the logical equipment address as it is. When the receive side determines that the destination address is the logical equipment address in accordance with the destined device number discrimination ID flag, whether information is addressed to the own device is determined in accordance with all or a

	Document ID	U	Title	Current OR
43	US 5870579 A	☒	Reorder buffer including a circuit for selecting a designated mask corresponding to an instruction that results in an exception	712/217
44	US 5859998 A	☒	Hierarchical microcode implementation of floating point instructions for a microprocessor	712/222
45	US 5848433 A	☒	Way prediction unit and a method for operating the same	711/137
46	US 5832297 A	☒	Superscalar microprocessor load/store unit employing a unified buffer and separate pointers for load and store operations	710/5
47	US 5828873 A	☒	Assembly queue for a floating point unit	712/222
48	US 5822574 A	☒	Functional unit with a pointer for mispredicted resolution, and a superscalar microprocessor employing the same	712/233
49	US 5822558 A	☒	Method and apparatus for predecoding variable byte-length instructions within a superscalar microprocessor	712/213
50	US 5819059 A	☒	Predecode unit adapted for variable byte-length instruction set processors and method of operating the same	712/213
51	US 5813033 A	☒	Superscalar microprocessor including a cache configured to detect dependencies between accesses to the cache and another cache	711/144
52	US 5805876 A	☒	Method and system for reducing average branch resolution time and effective misprediction penalty in a processor	712/234
53	US 5787474 A	☒	Dependency checking structure for a pair of caches which are accessed from different pipeline stages of an instruction processing pipeline	711/138
54	US 5768610 A	☒	Lookahead register value generator and a superscalar microprocessor employing same	712/23
55	US 5768555 A	☒	Reorder buffer employing last in buffer and last in line bits	712/216
56	US 5765016 A	☒	Reorder buffer configured to store both speculative and committed register states	712/23
57	US 5764946 A	☒	Superscalar microprocessor employing a way prediction unit to predict the way of an instruction fetch address and to concurrently provide a branch prediction address corresponding to the fetch address	712/239
58	US 5625789 A	☒	Apparatus for source operand dependendency analyses register renaming and rapid pipeline recovery in a microprocessor that issues and executes multiple instructions out-of-order in a single cycle	712/217

portion of the logical address, the own device logical address and the transmitter address so that only information addressed to the own device is acquired.

There is provided a packet transmission and receipt apparatus and a packet transmission and receipt method having an arrangement such that a low device for receiving the packet transmitted from the foregoing packet transmission and receipt apparatus to impart the destination when information is transmitted sets a multicast address in a case where the destination address has address indicating one device and multicast address when the destination address generated by the foregoing apparatus indicates a plurality of devices and sets unicast address when the destination address is one.

There is provided a packet transmission and receipt apparatus comprising another equipment address detection means for discriminating another equipment address with which wireless communication can be performed to detect the number of the devices; and simultaneous communication enabled device number determining section for determining the number of devices with which communication can be performed simultaneously with the detected devices to determine the maximum number. There is provided a method in which devices addresses of all or a portion of the destination devices and multicast address calculated from the address of the own device are set in an address field in which the maximum number of the devices determined by the simultaneously communication enabled device number determining section can be multicasted to transmit the same with the maximum number; and the receive side determines whether information is addressed to the own device in accordance with all or a portion of the maximum number, the multicast address, the destination address and the own equipment address of the own device imparted to the packet so that only information addressed to the own device is acquired.

The structure above is operated as follows:

The transmitter is assumed to be device X on a network as shown in FIG. 1. The device X intends to transmit data to devices A, B and C among a group of devices to which data can be transmitted. Note that each device knows the own address and addresses of the other devices. The device X calculates the multicast address from the addresses of the other devices and the own address, and then adds the multicast address and, if necessary, the transmitter address to a packet header having a fixed length when information is transmitted. In a case where a lower device receives the packet transmitted from the foregoing packet transmission and receipt apparatus and imparts the address when transmission is performed, the address is transmitted by setting the broadcast address.

In a case where information is transmitted to one device, the calculated multicast address is set to the equipment address of the destination device so that labor required to calculate the multicast address is omitted. In a case where address is imparted by the low device when information is transmitted, the address in the low device is set to be the broadcast address when transmission is performed.

The receiving side receives the transmitted packet to determine whether data is addressed to the own device in accordance with the multicast address imparted to the received packet header, the own address and the address of the transmitter, if necessary. As a result, the transmitter is able to perform multiple communication to a plurality of devices with one packet and without negotiation because the multicast address is imparted which can be obtained by only the calculations using the address of each device. When information is received, the packet destined to the own device is selectively received by only the calculation using the multicast address of the header of the received packet and the own address so that efficient multicast information transference is performed. If the address field for describing the multicast address is insufficient for the devices with which communication can be held, an address field for the maximum number of devices with which communication can be held simultaneously is secured. Then, the multicast address is calculated by a method similar to the foregoing. The receiving side is able to selectively receive the packet destined to the own device by the foregoing method in accordance with the address field length, the multicast address and the like described in the received packet.

Programs for executing the above methods and operating the above apparatuses may be stared in storage media.

Additional objects and advantages of the invention will be set forth in the description which follows, and in part will be obvious from the description, or may be learned by practice of the invention. The objects and advantages of the invention may be realized and obtained by means of the instrumentalities and combinations particularly pointed out in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate presently preferred embodiments of the invention and, together with the general description given above and the detailed description of the preferred embodiments given below, serve to explain the principles of the invention.

FIG. **1** is a conceptual view of a network;

FIG. **2** is a conceptual view of a packet structure;

FIG. **3** is a block diagram showing a communication control apparatus according to Embodiment 1 of the present invention;

FIG. **4** is a diagram showing a network of the communication control apparatus according to the present invention;

FIG. **5** shows a state of communication among terminal according to the present invention;

FIG. **6** shows terminal ID information according to Embodiment 1 of the present invention;

FIG. **7** shows information memorized in another terminal identifier memory section according to Embodiment 1 of the present invention;

FIG. **8** is a flow chart showing a process for setting an own terminal identifier according to Embodiment 1 of the present invention;

FIG. **9** is a block diagram showing a communication control apparatus according to Embodiment 4 of the present invention;

FIG. **10** shows terminal ID information according to embodiment 4 of the present invention;

FIG. **11** shows information memorized in another terminal memory section according to Embodiment 4 of the present invention;

FIG. **12** is a block diagram showing the communication control apparatus according to Embodiment 5 of the present invention;

FIG. **13** is a block diagram showing the communication control apparatus according to Embodiment 6 of the present invention;

FIG. **14** is a block diagram showing the communication control apparatus according to Embodiment 7 of the present invention;